REMARKS

Claims 1-18 are pending in the present application. Claims 16-18 have been added, and claims 1, 4, and 8 have been amended. No new matter has been added. Applicants respectfully request reconsideration of the claims in view of the following remarks.

Support for the amendments to claims 1, 4, and 8 is found at least at paragraph [0023] of the published application (Pub. No. US 2005/0235111 A1), which teaches that the cache controller attempts to update an external memory, via a dummy interface, in order to mirror the data that is stored in the data cache. Support for new claims 16-18 is found at least at paragraphs [0023] and [0029].

Claims 1, 3-6, 8, 9, and 11-13 have been rejected under 35 U.S.C. § 102(b) as assertedly being anticipated by U.S. Patent No. 5,829,038 to Merrell, et al. (hereinafter "Merrell").

Claim 1, as amended, requires:

> an interface external to the internal data cache and configured to receive cache mirror data from the processor chip.

Claim 8, as amended, requires:

> an interface external to the internal data cache and coupled between the processor chip and the external memory.

Claim 16, as amended, requires an:

> external memory interface . . . located outside the integrated circuit.

In the current Office Action, the Examiner identifies Merrell's hierarchical cache structure 15 as being the claimed external interface and notes that the previous claim language did not require that the interface be external to the processor chip. *See e.g.*, Office Action at 2, 3. As amended, claims 1 and 8 require that the interface is external to the internal data cache, and claim 16 requires that the interface be located outside the integrated circuit, which includes

the processor, internal data cache, and cache controller. Accordingly, Merrell's hierarchical cache structure 15 cannot be the claimed external interface.

Claim 1 further requires that:

> the interface [is] further configured to discard all the cache mirror data to be written to an external memory received from the processor chip so that cache mirror data is never written to external memory during operation of the processor chip.

Claim 4 requires:

> discarding the write instructions so that cache mirror data is never written to external memory during operation of the processing chip.

Claim 8 further requires that:

> the interface [is] further configured to receive internal data cache mirror data from the processor chip and discard all the internal data cache mirror data to be written to the external memory so that internal data cache mirror data is never written to external memory.

Claim 16 requires:

> discarding the cache mirror data write instructions at the external memory interface so that cache mirror data is never written to external memory during operation of the processor.

The Merrell reference does not disclose discarding data or write instructions so that cache mirror data is never written to external memory during operation of the processor. Instead, Merrell discloses a multi-level write-back cache in which data may be stored in multiple locations, such as a higher or lower cache line. Abstract. Merrell teaches that sometimes the cache line will not be written back to the memory subsystem (e.g. external memory). However, if the line no longer exists in any of the cache levels, then it will be written to the memory subsystem. Col. 2, lns. 10-13.

Data in Merrell's cache is always written to the memory subsystem or some other cache level at some point. For example, during the process illustrated in Figure 2, it is determined

whether the victim line is modified or clean (step 202). If that data has been mirrored in an associated line in a higher level cache or memory subsystem, then the victim line can be "evicted." Col. 3, lines 60-67. If the modified data has not been mirrored in an associated cache, it is first written back or mirrored before being evicted. Col. 4, lines 1-14. Accordingly, all data in the Merrill system must be mirrored from the cache at some point either before or during the cited "eviction" process. In the claimed systems and methods, the data is never mirrored and, therefore, this disclosure of Merrill does not anticipate the claim under § 102.

Similarly, the Klein, Handy and Stewart references fail to disclose that the cache data is never mirrored or written to external memory. Applicants again object to the proposed combinations under the Examiner's § 103 rejections and incorporate the arguments from Applicants' previous Amendments. Accordingly, Applicants respectfully submit that claims 1 to 16 are patentable over the cited references and should be passed to issue.

Claims 2, 3, 5-7, and 9-15 depend from claims 1, 4 and 8, respectfully and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

In view of the above, Applicants respectfully submit that the application is in condition for allowance and request that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicants request that the Examiner please contact Applicants' attorney at the address below. In the event that the enclosed fees are insufficient, please charge any additional fees required to keep this application pending, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

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